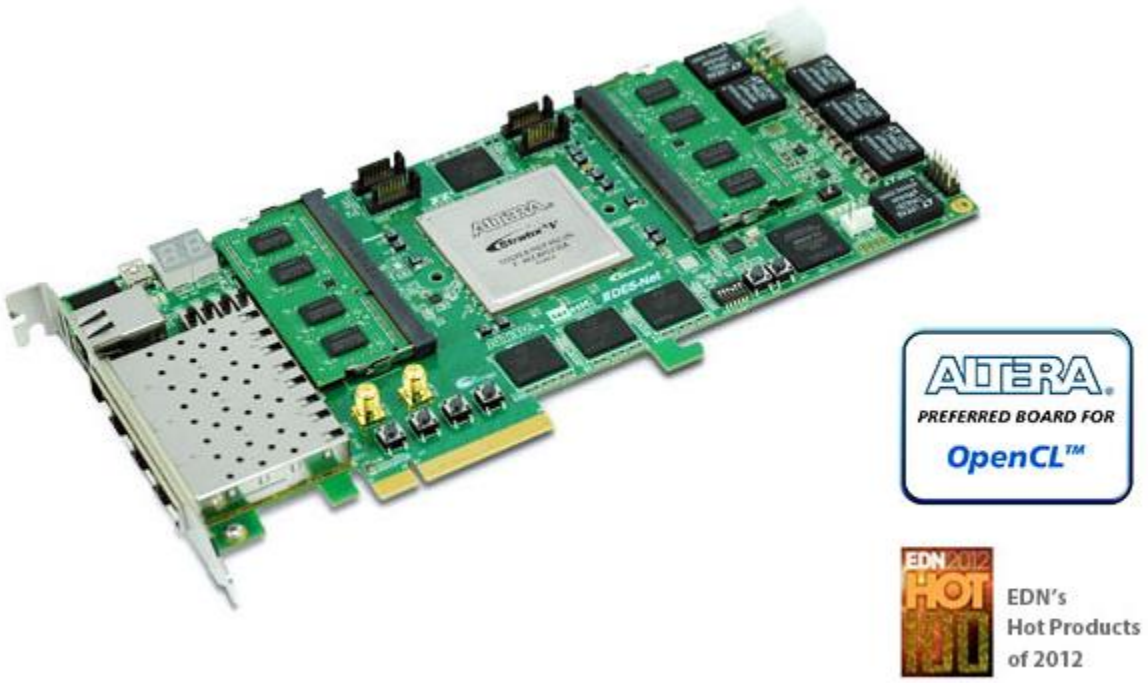
DE5-Net FPGA Development Kit

1. Overview



The Terasic DE5-Net Stratix V GX FPGA Development Kit provides the ideal hardware solution for designs that demand high capacity and bandwidth memory interfacing, ultra-low latency communication, and power efficiency. With a full-height, 3/4-length form-factor package, the DE5-Net is designed for the most demanding high-end applications, empowered with the top-of-the-line Altera Stratix V GX, delivering the best system-level integration and flexibility in the industry.

The Stratix® V GX FPGA features integrated transceivers that transfer at a maximum of 12.5 Gbps, allowing the DE5-Net to be fully compliant with version 3.0 of the PCI Express standard, as well as allowing an ultra low-latency, straight connections to four external 10G SFP+ modules. Not relying on an external PHY will accelerate mainstream development of network applications enabling customers to deploy designs for a broad range of high-speed connectivity applications. For designs that demand high capacity and high speed for memory and storage, the DE5-Net delivers with two independent banks of DDR3 SO-DIMM RAM, four independent banks of Cypress QDRII+ SRAM or functional compatible SRAMS provided by GSI and ISSI, high-speed parallel flash memory, and four SATA ports. The feature-set of the DE5-Net fully supports all high-intensity applications such as low-latency trading, cloud computing, high-performance computing, data acquisition, network processing, and signal processing.

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2. Specification

FPGA

FPGA
Altera Stratix® V GX FPGA (5SGXEA7N2F45C2)
FPGA Configuration
On-Board USB Blaster II or JTAG header for FPGA programming
Fast passive parallel (FPPx32) configuration via MAX II CPLD and flash memory

Memory

Memory
Two Independent DDR3 SODIMM Socket, Up to 8GB 800 MHz or 4GB 1066 MHz for each socket
Four Independent 550MHz SRAM, 18-bits data bus and 72Mbit for each
256MB FLASH

Communication

Communication Ports
Four SFP+ connectors
PCI Express (PCIe) x8 edge connector (includes Windows PCIe drivers)
One RS422 expansion header

Others

General user input / output:
4 LEDs
1 LED Array
4 push-buttons
4 slide switches
2 seven-segment displays
SMA clock input / output
On-Board Clock
50MHz Oscillator
Programmable oscillators Si570, CDCM61001 and CDCM61004
System Monitor and Control
Temperature sensor
Fan control
Power

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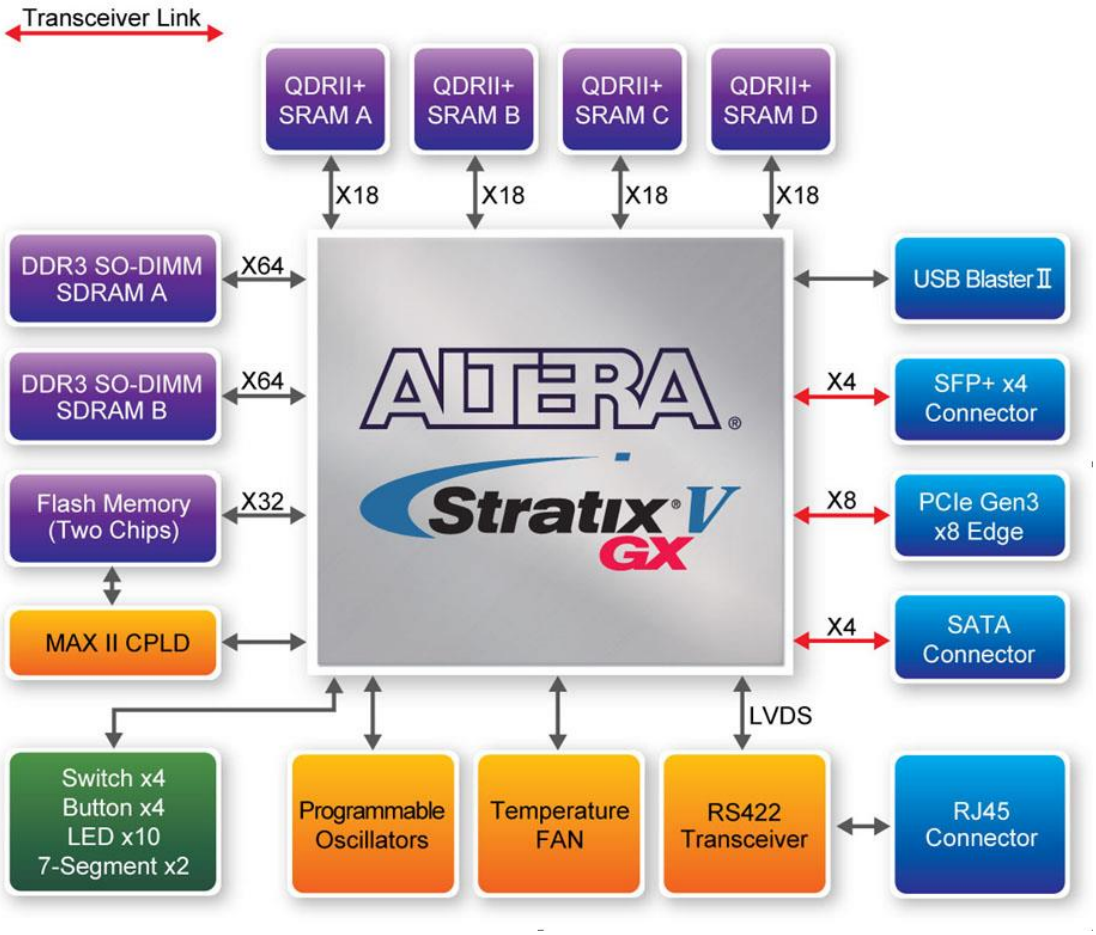
PCI Express 6-pin power connector, 12V DC Input
PCI Express edge connector power
Mechanical Specification
PCI Express standard height and 3/4-length

Block Diagram



3. Kit content

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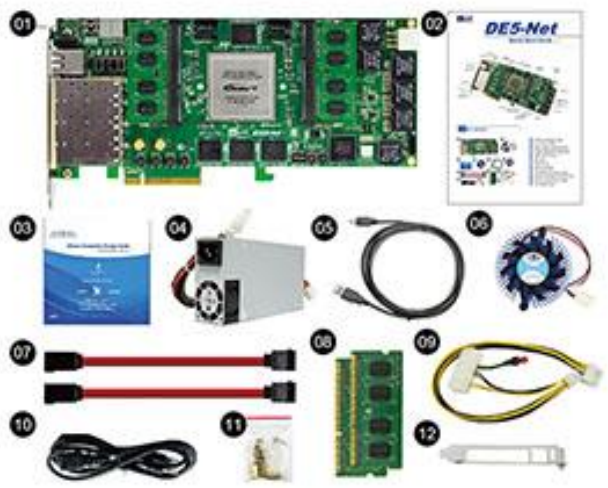
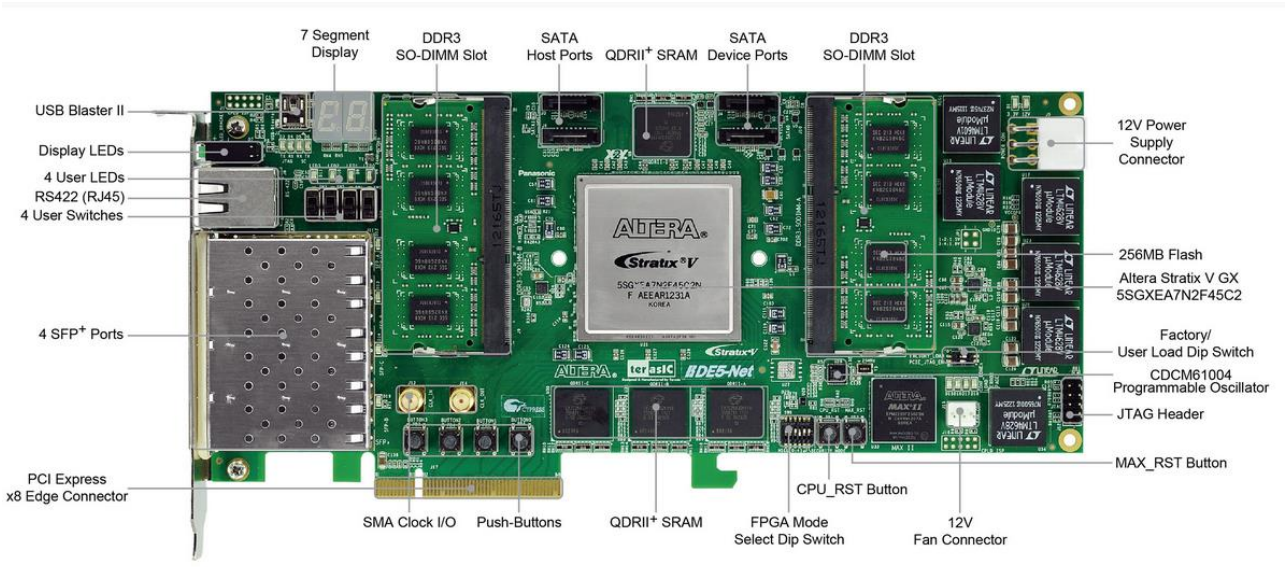


01 DE5-Net Development Board
02 DE5-Net Quick Start Guide
03 Altera Complete Design Suite DVD
04 Power Supply (250W)
05 USB to USB Mini Cable
06 Fan (Installed)
07 SATA Cable x2
08 DDR3 SO-DIMM x2
09 Power Cable (Attached to power supply)
10 AC Power Cord (Type B North American plug)
11 Screw and Copper Pillar Package
12 PCIe Bracket (Installed)

4. Application

The DE5-Net Stratix V FPGA Development Kit is perfectly suited for extreme high speed needs including cloud computing, high frequency trading, and security networks. Featuring an ultra-high bandwidth memory architecture, low-latency SFP+ interfaces, expandable memory, and PCIe communication, the DE5-Net allows for maximum flexibility in terms of low-power, speed, and performance.

5. Layout



*Cypress QDRII+ SRAM or functional compatible SRAMS provided by GSI (SigmaQuad-II+) and ISSI (QUADP).

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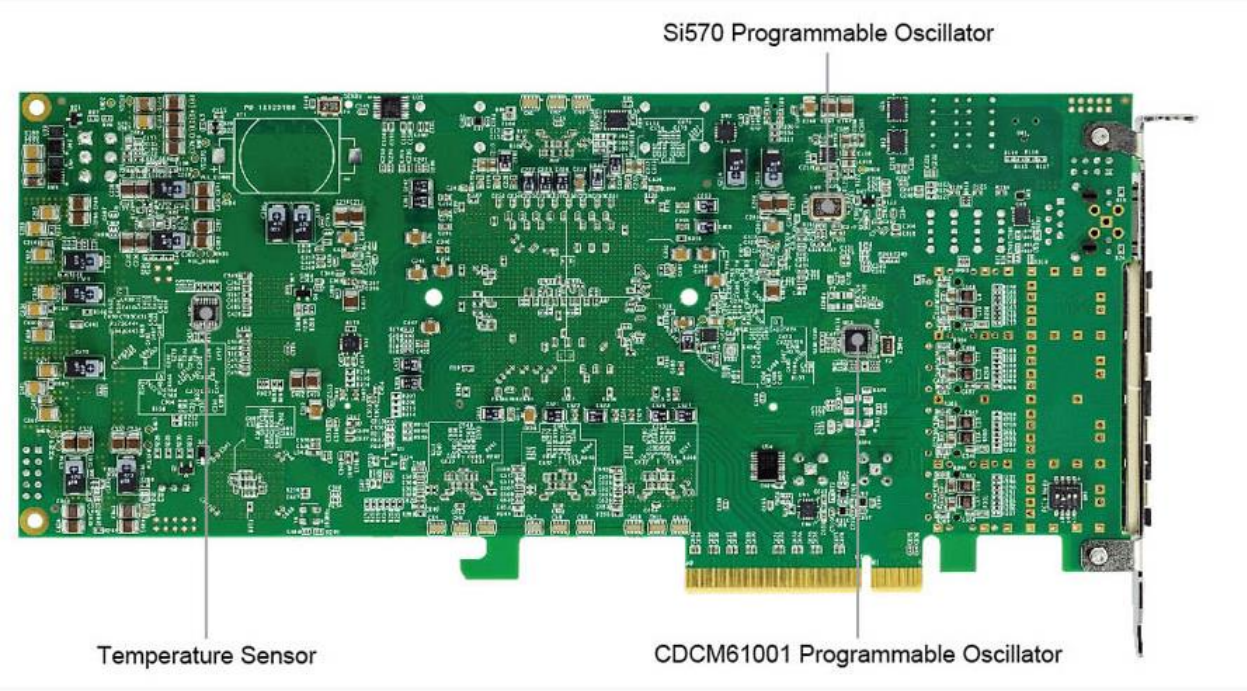

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